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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,147	07/16/2003	Robert Ian Gresham	18065	1214

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EXAMINER	
CAVALLARI, DANIEL J	
ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,147	GRESHAM, ROBERT IAN	
	Examiner	Art Unit	
	Daniel J. Cavallari	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/21/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-9 & 11 in the reply filed on 2/21/2006 is acknowledged.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 2/21/2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

The drawings are objected to for the following reasons:

- Figures 2A & 2B appear incorrectly drawn rendering the circuit inoperable. For example, but not limited to:
    - The isolation channels of the differential amplifiers for the 1st and 2nd input of Figure 2A do not contain a source attached to the collectors of the transistors as expected.
    - The supply voltages (Vdc) are drawn in figure 2B as the commonly used symbol for a capacitor and should be changed to represent a voltage source.

- The input 1 of Figure 2B is directly connected to itself. It appears that the lower input 1 should be tied to the gates of transistors (Q2 & Q3), which it is not.

The applicant should check the drawings for accuracy making sure those connections cited by the examiner as well as others are properly drawn.

- Figures 3 & 4 are of poor quality making it unclear what is being depicted. Furthermore, the physical transistor fabrication is presented at such a level to be illegible as it is unclear what is being depicted in those drawings and each and every component is failed to be labeled and described. The examiner suggests that Figures 3 & 4 be omitted.

Claim Objections

Claim 9 is objected to because of the following informalities:

- Claim 9 recites the limitation "...providing coupling between the input and output of the circuit..." however "...at least two inputs..." is disclosed therefore it is unclear what is meant by "the input". The claim will be examined as best understood to mean "an input".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 recites the limitation of "at least one third transistor for providing a control bias for selecting either the transmit channel or the isolation channel" however, the applicant only teaches a configuration comprising of two transistors (i.e. 241', 240, See Figures 2A & 2B) which are used to provide a control bias to select either the isolation or transmit channel on a given side of the switch (Section 1 or Section 2). It is unclear how a single transistor could perform such selection.

The claim will be examined as best understood to mean two transistors.

Claim 5 recites the limitation of "wherein the at least one first transistor comprises three transistors and the at least one second transistor comprises three transistors." Drawings 2A & 2B show the "first transistor" which comprises the isolation channel as being comprised of transistors (Q1 & Q2) for the first circuit portion and (Q11 & Q12) for the second circuit portion. There is no disclosure of the isolation channel comprising of

three transistors therefore it is unclear how the isolation channel could comprise of three transistors.

Because of the 112 problems, no art can be applied to Claim 5.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 appears improperly dependant on Claim 1 as claim 11 recites "The receiver apparatus of claim 1" however claim one is "A switching circuit...". It appears claim 11 was meant to be dependant on claim 10.

Because of the 112 problems, no art can be applied to claim 11.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, 6, 7, & 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Miki et al. (US 5,396,131).

In regard to Claims 1, 6, & 9

Miki et al. (hereinafter referred to as Miki)

- A first circuit portion (401) corresponding to a first input port, read on by VA1 & VA2 (Channel 1) (See Figure 10).
- A second circuit portion (402) corresponding to a second input port, read on by the input to transistor gates 301' & 302' (Channel 2) (See Figure 10).
- An output port, read on by I_{10} & I_{20} (See Figure 10).
- Wherein each of the first and second circuit portions includes at least one first transistor, read on by a first differential amplifier (301 and 301') providing a portion of an isolation channel , at least a second transistor, read on by a second differential amplifier (303 and 303') providing a portion of a transmit channel, and two third transistors for providing a control bias which selects an input, read on by 305 & 306 and its equivalent in circuit 402 (See Figure 10).

In regard to Claim 3

- The third transistors (305, 306, and corresponding transistors for circuit 402) of the first and second portions provides a control bias for selecting which of the first and second input ports are coupled to the output port (I_{10} & I_{20}).

In regard to Claim 4 & 7

- The at least one first transistor (301) comprises two transistors (301 & 302) having emitters coupled to each other and coupled to a collector of the third transistor (305) (See Figure 10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miki et al. and Limberg (US 3,798,376).

Incorporating all arguments above of the switching device taught by Miki, Miki further teaches the use of solid state devices (See Figure 10), but fails to explicitly teach the circuit formed on an integrated circuit.

Limberg teaches solid state components integrated on an integrated circuit (See Column 2, Lines 13-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the switching circuit of Miki into an integrated circuit as taught by Limberg. The motivation would have been the reduced size and weight,

increased reliability and economic advantages offered by integrated circuits as opposed to discrete components (See Limberg, column 2, Lines 13-26).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Kurogouchi et al. (US 6,466,064)
- Taniguchi et al. (US 6,784,743)
- Dick (US 5,977,827) teaches the use of two differential amplifiers in a single circuit (See Figure 2)
- Gresham (US 6,987,419) teaches a single channel microwave switch.
- Morf et al. (US 2004/0263236 A1) teaches a multi-channel switch.\
- Sone (US 5,510,734)
- Jain (US 6,819,201)
- McClure (US 5,487,048)
- Friesen (DE 4,235,909 A1)
- Fenk et al. (US 5,652,543)
- Hasegawa (US 6,188,339)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Cavallari whose telephone number is (571)272-8541. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel Cavallari

May 11, 2006

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SUPERVISORY PATENT EXAMINER
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